an Intel company

2.5 Gbit/s Clock and Data Recovery and 1:16 DeMUX GD16524

General Description

The GD16524 is a high performance monolithic integrated multi-rate *Clock and Data Recovery* (CDR) device applicable for optical communication systems including:

- SDH STM-16 / 4 / 1
- SONET OC-48 / 12 / 3
- Gigabit Ethernet

The GD16524 features:

- Limiting input amplifier.
- Analogue peak level detection circuit.
- Digital Loss Of Signal (LOS) monitor circuit with four selectable threshold settings.
- Consecutive Identical Binary Digit alarm output.
- 1:16 de-multiplexer.

GD16524 can be switched “on-the-fly” to and from 2.488 Gbit/s, 1.244 Gbit/s, 622.08 Mbit/s, and 155.52 Mbit/s. GD16524 also supports up to 7% overhead, allowing for 2.66 Gbit/s data transfer.

The device also features an additional high-speed data input for serial loop-back diagnostic tests.

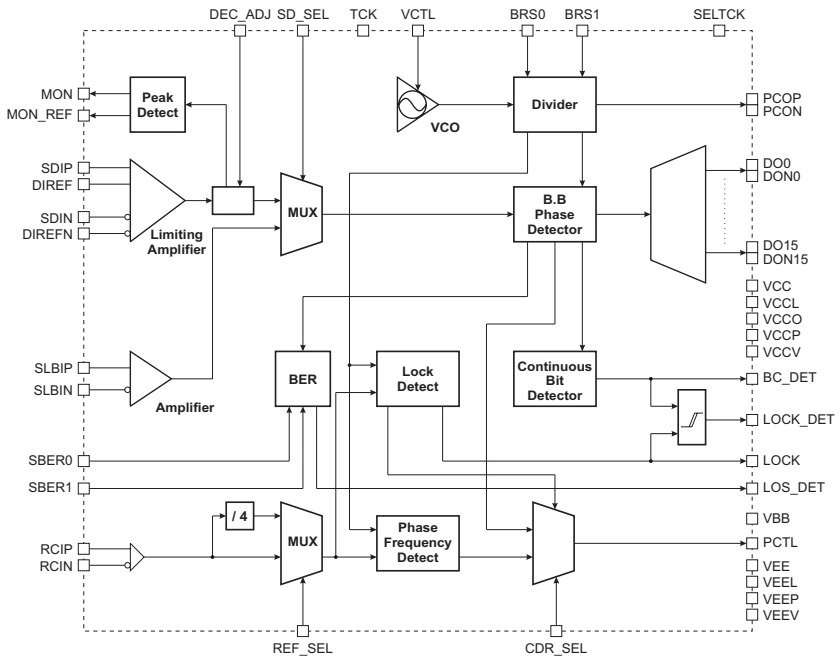
The CDR contains all circuits needed for reliable acquisition and lock of the VCO phase to the incoming data-stream. The electrical input sensitivity is better than 8 mV (BER <10^{-10}).

The device exceeds all ITU-T and Bellcore IEEE jitter requirements when used with the recommended loop filter, according to Figure 3 (jitter tolerance, -transfer and -generation).

The output clock (2.488 GHz when STM-16 data input is selected) is maintained within 500 ppm tolerance of the reference frequency in the absence of data.

The integrated 1:16 de-multiplexer with differential LVPECL outputs provides a simple interface to system ASICs.

The GD16524 is available in a 100 pin TQFP package (14 × 14 mm) with heat slug on bottom surface.



Features

- Exceeds ITU-T and Bellcore requirements of Jitter Transfer, Generation and Tolerance.
- Integrated Limiting amplifier.
- On-the-fly multi-bit-rate operation 7% overhead data rate capability.
- Digital LOS monitor and alarm output.
- Bit Consecutive Detect output.
- Multi-rate data input.
- Differential CML data input with internal 50 Ω load termination.
- Integrated 1:16 DeMUX with LVPECL outputs.
- Control inputs are LVTTL.
- Reference clock selectable:
  - 155.52 MHz
  - 38.88 MHz
- High-speed serial loop-back input.
- Single supply operation: +3.3 V
- Power dissipation: 800 mW (typ.)
- Available in a 100 pin TQFP package (14 × 14 mm) with heat slug on bottom surface.

Applications

- Clock and Data Recovery for optical communication systems including:
  - SDH STM-16
  - SONET OC-48
  - Gigabit Ethernet

Functional Details

The main application of the GD16524 is as a receiver for optical communication systems:

- SDH STM-16
- SONET OC-48
- Gigabit Ethernet

It integrates:

- a Limiting Amplifier
- Serial loop-back input
- a Voltage Controlled Oscillator (VCO)
- a Lock Detect Circuit
- a Frequency Detector (PFD)
- a Continuous Bit Detector
- a Bang-Bang Phase Detector
- an integrated 1:16 DEMUX
- Digital LOS Alarm

into a *Phase Locked Loop* (PLL) - based multi-rate clock and data recovery circuit with differential CML data inputs and LVPECL differential data and clock outputs.

VCO

The VCO is a low noise LC-type differential oscillator with a tuning range from 2.4 to 2.7 GHz. Tuning is done by applying a voltage to the VCTL pin.

Lock Detect Circuit

The internal lock detect circuit continuously monitors the difference between the reference clock and the divided VCO clock. If the reference clock and the divided VCO frequency differ by more than 500 ppm, it switches the PFD into the PLL in order to pull the VCO back inside the lock-in range. This mode is called **the acquisition mode.**

The PFD is used to ensure predictable lock up conditions for the GD16524 by locking the VCO to an external reference clock source. It is only used during acquisition and pulls the VCO into the lock-in range where the Bang-Bang phase detector is capable of acquiring lock. The PFD is made with digital set/reset cells giving it a true phase and frequency characteristic.

Once the VCO is inside the lock-range the lock-detection circuit switches the Bang-Bang phase detector into the PLL in order to lock to the data signal. This mode is called **CDR mode**.

If the divided VCO frequency differs from the reference frequency by ±500 ppm, i.e. due to data loss, the internal lock detect circuit will give a stable output clock during a loss of data condition.

The reference clock to the PFD is at 1/64 of the STM16 / OC-48 data rate. By using REF_SEL pin the reference clock input (RCIP/N) can be chosen to use a 155.52 MHz or 38.88 MHz differential PECL reference clock. The reference clock frequency is independent of the chosen data rate.

The BC_DET Signal

An internal circuit monitors input data transitions and gives a BC_DET output signal which is asserted if more than 256 consecutive identical bits, 0s or 1s, are detected.

BC_DET will be de-asserted only after approximately 16 bit transitions are detected within a time period proportional to the selected data rate (50 ns at STM 16 / OC-48).

Bang-Bang Phase Detector

The Bang-Bang phase detector is used in **CDR mode** as a true digital type detector, producing a binary output. It samples the incoming data twice each bit period: once in the transition of the (previous) bit period and once in the middle of the bit period. When a transition occurs between 2 consecutive bits - the value of the sample in the transition between the bits will show whether the VCO clock leads or lags the data. Hence the PLL is controlled by the bit transition point, thereby ensuring that data is sampled in the middle of the eye, once the system is in CDR mode. The external loop filter components control the characteristics of the PLL.

The binary output of either the PFD or the Bang-Bang phase detector (depending of the mode of the lock-detection circuit) is passed to a charge pump which can sink or source current or tristate. The output of the charge pump is filtered by the recommended external loop filter (for details, please refer to Figure 3) and controls the tuning voltage of the VCO.

As a result of the continuous monitoring of the lock-detect circuit, the VCO frequency never deviates more than 500 ppm from the reference clock before the PLL is considered to be 'Out of Lock'. Hence the acquisition time is predictable and short and the output clock PCOP/N is always kept within the 500 ppm limits, ensuring safe clocking of downstream circuitry.

The LOCK_DET Signal

The LOCK_DET signal is a status output, which monitors the status of the internal lock detect circuit of the GD16524 CDR logic and the output of the BC_DET circuit.

LOCK_DET is asserted (set HIGH) if the VCO frequency differs from the reference frequency by ±500 ppm. This ' out of lock' condition is detected by the internal Lock Detect circuit described previously. LOCK_DET is also asserted in the case of the absence of data, which is detected by the BC_DET circuit within the reaction time of the internal PLL lock detect system.

If data is absent, the divided VCO frequency will drift away from the reference frequency until they differ by ±500 ppm. The internal Lock Detect logic will alternate between CDR and acquisition mode until data returns, enabling the GD16524 to acquire lock and function in CDR mode.

The LOCK_DET signal, however, will remain asserted until BC_DET is de- asserted and the internal lock detect circuit is operating in CDR mode.

The CDR circuitry of the GD16524 has been fine-tuned to provide an accurate stable clock output from the VCO when data is present. Due to the precise nature of the internal VCO, when data is absent the clock output frequency will drift slowly from the recovered clock frequency until an out of lock condition is detected. The time taken for the GD16524 to go 'out of lock' in the absence of data will typically be at least 3 ms, unless an external circuit is used to pull the VCO frequency away from the reference frequency.

When loss of data is detected, i.e. BC_DET is asserted, or the divided VCO frequency differs from the reference frequency by ±500 ppm, LOCK_DET is asserted and the internal lock detect circuit switches to acquisition mode. This will give a stable output clock during a loss of data condition.

When BC_DET is de-asserted and the divided VCO frequency is within 500 ppm of the reference frequency, LOCK_DET will be de-asserted within 500 μs, independent of selected data rate.

LOS_DET

The Loss Of Signal DETection (LOS_DET) alarm output is low during normal operation.

The LOS_DET signal is the output from a digital Bit Error Flag (BEF) circuit which monitors the number of false bit transitions in the data signal. A internal flag is raised if the number of false transitions is above a predefined level, i.e. if the Bit Error Rate (BER) is above a predefined level.

This has been realised with a counter counting the false bit transitions. If this counter runs out within a time period the BEF flag is set. The length of the counter may be set by external select signals (SBER0 and SBER1). The time period that the false errors are counted within is 64 kbit/s corresponding to 26 μs at STM 16 / OC-48 data rate. The length of the counter may be set to detect approximate bit error rates of 0.5E-3, 1E-3, 2E-3 or 4E-3.

The input to the BEF circuit is derived from Bang-Bang detector sample data. As discussed above, the Bang-Bang detector samples the incoming data twice each bit period, once at the transition and once in the middle of the eye. If the value of the samples in the middle of the eye for two consecutive bits is equal but the value of the transition sample is different then a bit error has occurred.

As the BEF system detects false bit transitions between two consecutive bits, only bit errors due to high frequency noise are detected. Therefore there will not be a 1:1 correlation between the actual BER of the signal and the number of errors detected by the BEF system. However the actual bit error rate is correlated to the number of errors detected in the BEF system. This means that by choosing the appropriate counter length, it will be possible for the BEF system to set the BEF flag at a user selectable bit error rate.

Once the LOS_DET signal has been asserted, it will be de-asserted only when the BER is less than ¼ of the set rate for a period which is proportional to the selected data rate. (at least 125 μs at STM16 / OC-48).

Peak Level Monitor

An integrated analogue peak level detector circuit continuously monitors the input data voltage swing.

The output from this circuit is conditioned and is available as an analogue output signal at the MON pin.

Data Inputs

Limiting Amplifier
The limiting input amplifier is a high performance input data signal conditioning buffer with sensitivity better than 8 mV. Data input is CML.

The inputs may be either AC or DC coupled. In both cases input termination is made through pins DIREF / DIREFN. If the inputs are AC coupled the amplifier features an internal offset cancelling DC feedback. Notice that the offset cancellation will only work when the input is AC-coupled as shown in the Figures on page 4.

The limiting amplifier inputs are operational when the SD_SEL input is connected to a logic high (VCC).

Alternatively, the high-speed serial loopback input can be selected by connecting SD_SEL to a logic low (VEE) to allow loop-back diagnostic testing of the system.

DEC_ADJ
The DEC_ADJ input can be used to compensate for input data with a non-symmetric duty cycle, allowing control over the DC bias level of the limiting amplifier output. The DC bias point can be steered up or down by an external potentiometer. By this means the optimum data sampling point of the Bang-Bang phase detector can be achieved for duty cycles of 30% to 70%. If the DEC_ADJ pin is unconnected the DC bias will default to an internally set level optimised for input data with a 50% duty cycle.

Peak Level Monitor (MON and MON_REF)
The MON and MON_REF pins can be used to indicate the peak level of input data. An output voltage is available at the MON pin, which is proportional to the peak level of the input signal. MON_REF is an internally generated fixed reference voltage. The difference between the value obtained at the MON pin and the value of MON_REF indicates the peak input data signal level.

Application data pertaining to use of MON, MON_REF and DEC_ADJ is available from GIGAs Application Department.

Bit Order

The first bit of the received serial data stream is demultiplexed to DO0, the second to DO1 and the last received bit in a 16 bit frame to DO15.

Outputs

Following the CDR logic the data is demultiplexed to 16 differential (LVPECL) data at 155.52 Mbit/s (STM-16 data rate operation selected) and output together with a differential 155.52 MHz clock. The clock outputs are also LVPECL.
The clock output frequency is related to the selected input data rate and demultiplexed data output bit rate.

An internally generated output data reference voltage (VBB) is also provided. See Figure 6 on page 4.

Package

The GD16524 is provided in a 100 pin TQFP package (14 × 14 mm) .

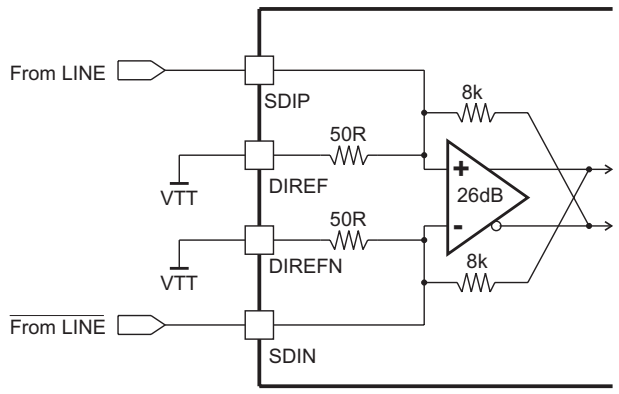


Figure 1. *DC Coupled Input (Ignoring internal offset compensation). Note 1.*

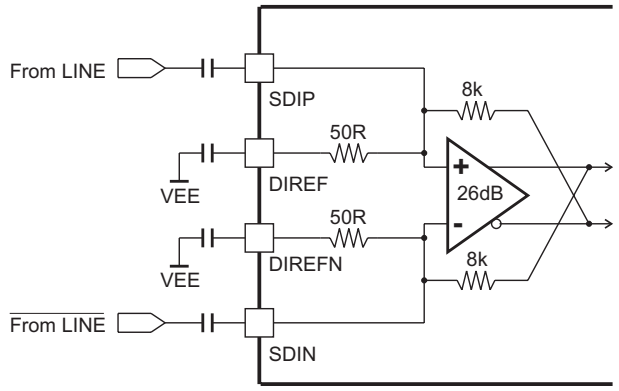


Figure 2. *AC Coupled Input (Using internal offset compensation). Note 1.*

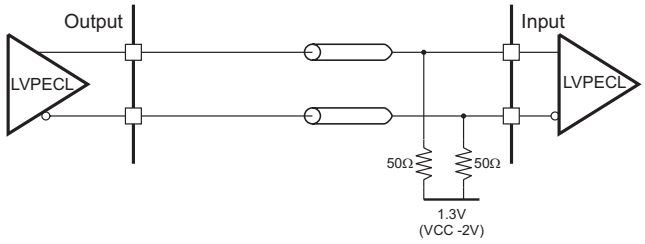


Figure 4. *DC Coupled Clock Outputs*

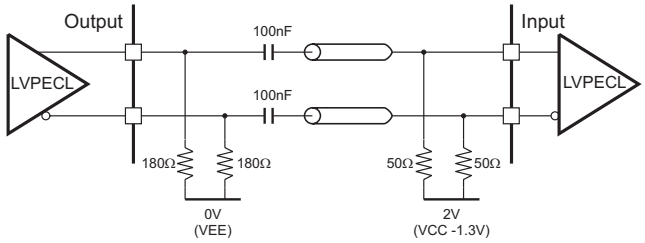


Figure 5. *AC Coupled Clock Outputs*

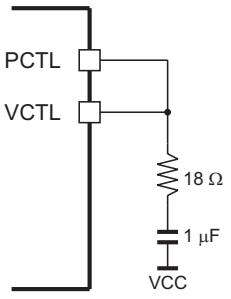


Figure 3. *Recommended Loop Filter*

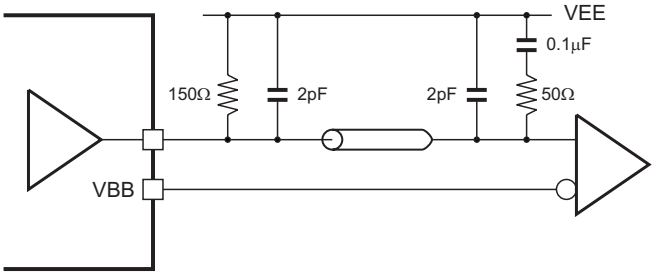


Figure 6. *Optional Single-ended Data Outputs*

Note 2: "2 pF" capacitor does not include PKG and on-chip stay capacitance. "150 Ω to GND" can be replaced by "50 Ω to VCC -2 V".

Note1 : VTT depends on the termination requirements of the previous stage and the resulting input amplitude. VTT can typically be connected to VCC potential.

Pin List

Mnemonic:	Pin no.:	Pin Type:	Description:
SDIP, SDIN	12, 10	CML IN	Differential AC or DC coupled 2.5 Gbit/s, 1.25 Gbit/s, 622 Mbit/s or 155 Mbit/s Data input.
DIREF, DIREFN	13, 9	Termination	Termination for SDIP and SDIN. Normally terminated with 50 Ω through 47 nF. For DC connected inputs connect to reference voltage via 50 Ω.
SLBIP, SLBIN	18, 17	CML IN	Differential Loop-Back Data inputs.
DO0 DON0 DO1 DON1 DO2 DON2 DO3 DON3 DO4 DON4 DO5 DON5 DO6 DON6 DO7 DON7 DO8 DON8 DO9 DON9 DO10 DON10 DO11 DON11 DO12 DON12 DO13 DON13 DO14 DON14 DO15 DON15	68, 67 66, 65 64, 63 62, 61 59, 58 57, 56 55, 54 53, 52 49, 48 47, 46 45, 44 43, 42 40, 39 38, 37 36, 35 34, 33	LVPECL OUT	Differential output data. Demultiplexed in the order DO0, DO1...DO15, with DO0 as the first received bit.
PCOP, PCON	70, 73	LVPECL OUT	Differential Clock output. Output frequency is related to selected input data bit rate. i.e. 155.52 MHz with 2.488 Gbits input data rate.
RCIP, RCIN	85, 83	PECL IN	Differential 155.52 MHz or 38.88 MHz reference clock input.
DEC_ADJ	14	ANL IN	Decision level adjust.
VCTL	97	ANL IN	VCO voltage control input.
MON	15	ANL OUT	Input data level monitor output.
MON_REF	16	ANL OUT	Input data level monitor reference voltage.
PCTL	91	ANL OUT	Charge pump control.
VBB	72	ANL OUT	Reference voltage output for parallel data.
REF_SEL	87	LVTTL IN	Reference CLK Frequency Select. 0 155.52 MHz 1 38.88 MHz
CDR_SEL	71	LVTTL IN	Clock and Data recovery set-up. 0 Auto lock, 500 ppm 1 Manual Phase Freq. detector PFC
BRS0, BRS1	88, 89	LVTTL IN	Multi-rate Data input select. BRS0 BRS1 Input 0 0 1.25 Gbit/s 0 1 155 Mbit/s 1 0 622 Mbit/s 1 1 2.5 Gbit/s
SBER0, SBER1	22, 23	LVTTL IN	BER select inputs. SBER0 SBER1 0 0 0.5×10^{-3} 0 1 1×10^{-3} 1 0 2×10^{-3} 1 1 4×10^{-3}
TCK	94	LVPECL IN	Leave open for normal operation. Only used at DC test.
SD_SEL	20	LVTTL IN	Data input Loop-Back or Limiting amplifier select. 0 Loop-Back inputs 1 Limiting Amplifier inputs
SELTCK	93	LVTTL IN	Test-clock select. Leave open for normal operation. Only used for test purposes.

Mnemonic:	Pin no.:	Pin Type:	Description:
LOCK	77	PCMOS OUT	A high level indicates that the PLL is locked to the incoming serial data. A low level indicates out of lock. When the GD16524 cannot acquire lock to the serial data this signal switch between ”0" and “1"
LOCK_DET	28	PCMOS OUT	Valid data loss alarm output. Asserted when the divided VCO frequency deviates more than 500 ppm from reference frequency, or BC_DET asserted.
LOS_DET	27	PCMOS OUT	Loss Of Signal alarm output.
BC_DET	26	PCMOS OUT	Bit consecutive detect output.
VEE	2, 19, 24, 29, 74-76, 86, 92	PWR	Negative supply voltage.
VEEL	8, 11	PWR	Negative supply for Limiting Amplifier.
VEEP	95	PWR	Negative supply for Charge Pump.
VEEV	100	PWR	Negative supply for VCO.
VCC	3-5, 21, 25, 30, 31, 78-82, 84, 90, 98, 99	PWR	Positive supply voltage.
VCCL	6, 7	PWR	Positive supply for Limiting Amplifier.
VCCO	32, 41, 50, 51, 60, 69,	PWR	Positive supply for Output.
VCCP	96	PWR	Positive supply for Charge Pump.
VCCV	1	PWR	Positive supply for VCO.
Heat slug			Connected to VEE.

Pin Outline

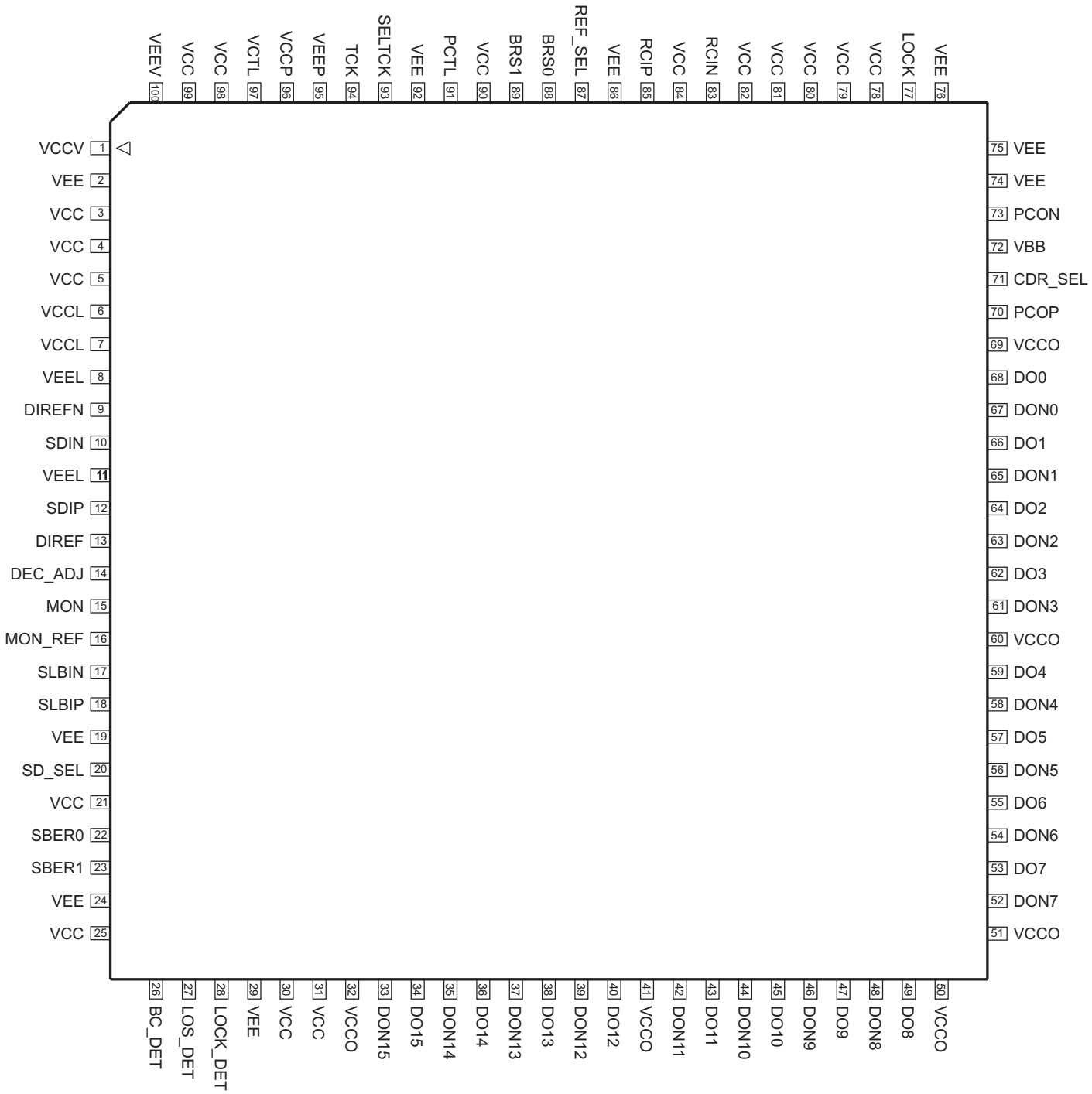


Figure 7. *Package Pinout, 100 pin. Top View.*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table are referred to V_{EE} .
All currents in the table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{CC}	Power supply		-0.5		6	V
V_I	Applied voltage (all inputs)		-0.5		V_{CC} +0.5	V
V_O	Applied voltage (all outputs)		-0.5		6.0	V
$V_{IO\ ESD,CML}$	Static Discharge Voltage	Note 1	500			V
$I_{O\ PCMOS}$	PCMOS output source current		-250		250	µA
$I_{O\ PCMOS}$	PCMOS output sink current		-250		250	µA
$I_{O\ PECL}$	PECL output source current				50	mA
$I_{O\ CHAP,\ LCAP}$	Charge pump output current		-250		250	µA
T_O	Operating temperature	Case	-40		+110	°C
T_S	Storage temperature		-65		+125	°C

Note 1: Human body model (100 pF, 1500 Ω) MIL 883 std.

DC Characteristics

T_{CASE} = -40 °C to +85 °C. Appropriate heat sink may be required. Device is DC tested in the temperature range 0 °C to 85 °C. Specifications from –40 °C to 0 °C are guaranteed by design and evaluated during the engineering test.
V_{CC} = 2.97 V to 3.6 V.

All voltages in the table are referred to V_{EE}.
All input signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

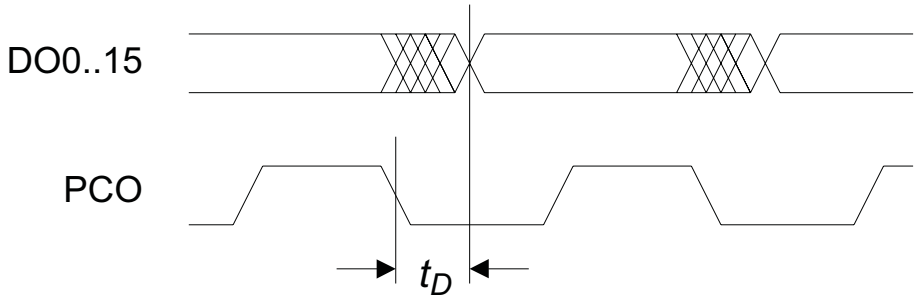
Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{CC}	Supply voltage		+2.97	+3.3	+3.6	V
I_{CC}	Supply current				250	mA
P_{DISS}	Power dissipation			800	900	mW
$V_{IH\ PECL}$	PECL-input HI voltage		V_{CC}-1.17		V_{CC} -0.87	V
$V_{IL\ PECL}$	PECL-input LO voltage		V_{CC}-2.01		V_{CC} -1.47	V
$I_{i\ PECL}$	PECL-input current	$V_{IH\ MAX}$ to $V_{IL\ MIN}$	-25		+150	µA
$V_{OH\ PECL}$	PECL-output HI voltage		V_{CC}-1.02		V_{CC} -0.89	V
$V_{OL\ PECL}$	PECL-output LO voltage		V_{CC}-2.00		V_{CC} -1.60	V
$I_{O\ VBB}$	VBB-output current		0.1		3.0	mA
$V_{IH\ LVTTL}$	LVTTL-input HI Voltage	Note 2	2.0		V_{CC}	V
$V_{IL\ LVTTL}$	LVTTL-intput LO Voltage	Note 2	0.0		0.8	V
$I_{IH\ LVTTL}$	LVTTL-input HI Current	Note 2			50	µA
$I_{IL\ LVTTL}$	LVTTL-input LO Current	Note 2	-500			µA
$V_{OH\ PCMOS}$	PCMOS-output HI Voltage	Note 1		V_{CC} -300		mV
$V_{OL\ PCMOS}$	PCMOS-output LO Voltage	Note 1		V_{EE} +300		mV
I_{VCTL}	VCTL leakage current	$V_{EE}<V_{VCTL}<V_{CC}$-1	-30			µA
$I_{OH\ CHAP}$	Charge pump output source current			100		µA
$I_{OL\ CHAP}$	Charge pump output sink current			-100		µA

Note 1: The PCMOS output is based on GIGA's Charge Pump output cell.
Note 2: All LVTTL inputs have an internal 16 kΩ pull-up resistor giving a default logic 1 input when unconnected.

AC Characteristics

T_{CASE} = -40 °C to +85 °C. Appropriate heat sink may be required. Device is AC tested in the temperature range 0 °C to 85 °C. Specifications from –40 °C to 0 °C are guaranteed by design and evaluated during the engineering test.
V_{CC} = 2.97 V to 3.6 V.

All data given below is reference to STM-16 / OC-48 input data rate unless otherwise stated.



Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT.:
J_{TRF}	Jitter Transfer		See Figure 8 on page 11			MHz
J_{TOL}	Jitter Tolerance Note 1		See Figure 9 on page 11			UI_{P-P}
Jpeak	Jitter Peaking				0.08	dB
J_{GEN}	Jitter Generation	Note 2		5	7-8	mUI_{RMS}
t_R / t_F	Rise/Fall Times DO0..15	20% - 80 %	400		900	ps
R_{CAPT}	Capture Range		-500		500	ppm
t_A	Acquisition Time	2^{23} -1 PRBS		50	500	µs
L_{CID}	Consecutive Identical Bits Sustained by PLL	# of bits with no transition	400	1000		bits
L_{LOCK_DET}	LOCK_DET low to high	SDI off	103		130	ns
	LOCK_DET high to low	SDI on	412		514	µs
L_{LOS_DET}	LOS_DET low to high	BER above preset level			26	µs
	LOS_DET high to low	BER below preset level	131		316	µs
F_{RCI}	Reference Clock 1 Reference Clock 1			155.52 38.88		MHz MHz
t_D	Output Phase Delay		-0.3		+0.3	ns
$D_{DUTY\ PDO}$	Output Data Duty Cycle Deviation		45		55	%
$C_{DUTY\ PCO}$	Output Clock Duty Cycle Deviation		45		55	%
	Decision Level Adjustable Range	Maximum swing = 100%	30	50	70	%
	Decision Level Deviation		-3		+3	%
D_C	Input Data / RCI Frequency Deviation	Note 3	-200		200	ppm
$C_{DUTY\ RCI}$	Reference Clock Duty Cycle Deviation	Vthr = -1.3 V	40		60	%
F_{VCO}	VCO Tuning Range		2.4		2.7	GHz
f_{IN}	Necessary Input Amplitude to Stay Locked	Note 4		2	3	mV
S_{ABS}	Absolute Input Sensitivity	BER 1E-10, Note 4		5	8	mV

Note 1: 1 UI_{P-P} = 402 ps
Note 2: Signal applied to both inputs.
Note 3: Maximum allowable deviation between reference clock and divided VCO clock when locked to data.
Note 4: Differential 2^{23} -1 PRBS jitter free input data.

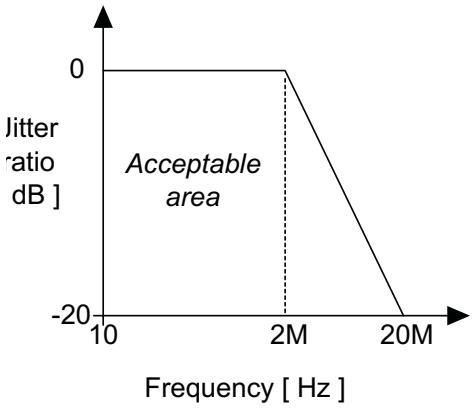


Figure 8. *Jitter Transfer (STM-16/OC-48).*

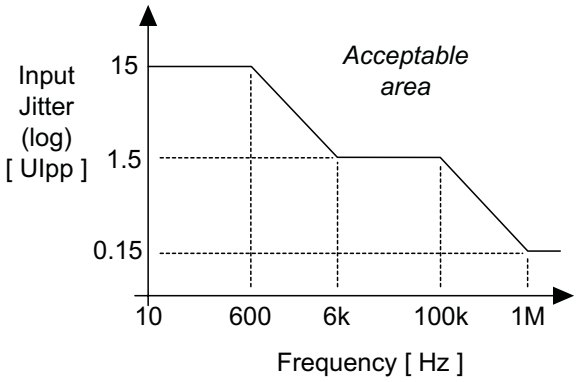
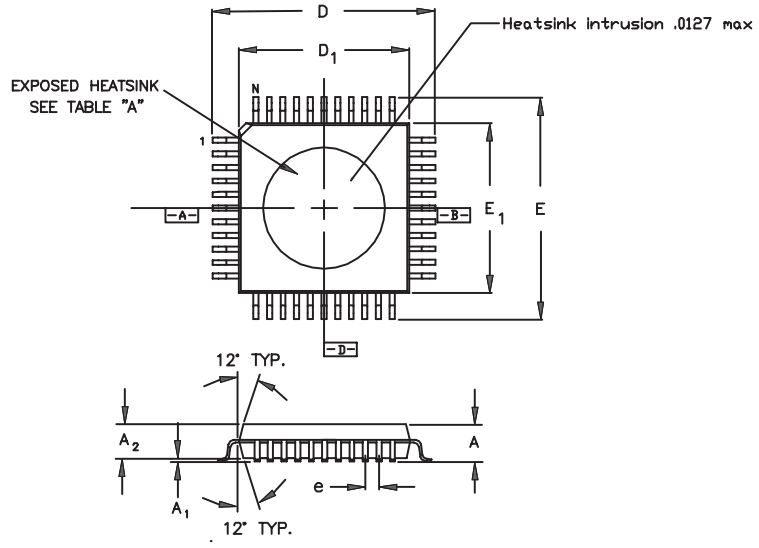


Figure 9. *Jitter Tolerance (STM-16/OC-48).*

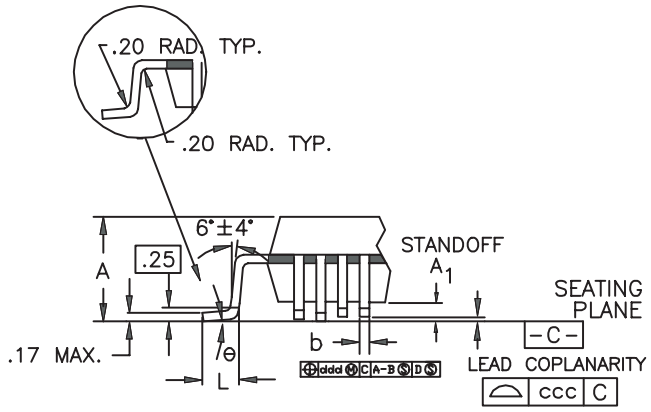
Package Outline



BODY + 2.00 mm FOOTPRINT		
	LEADS	100L–1.4 THK.
DIMS.	TOL.	
A	MAX.	1.60
A_1		.05 MIN./.15 MAX.
A_2	±.05	1.40
D	±.20	16.00
D_1	±.05	14.00
E	±.20	16.00
E_1	±.05	14.00
L	+.15/–.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°–7°
ddd	MAX.	.08
ccc	MAX.	.08

TABLE "A"

INTERPOSER RING SIZE	EXPOSED HEATSINK DIA.
6.10x6.10 / 7.11x7.11	6.60 ±.50



NOTES:
1) ALL DIMENSIONS IN MM.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOL. AS INDICATED.
3) L/F: EFTEC 64T COPPER OR EQUIVALENT, 0.127 MM (.005") OR 0.15 MM (.006") THICK.
4) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, AT 0.25 ABOVE THE SEATING PLANE.

Figure 10. *Package 100 pin TQFP. All dimensions are in mm.*

Device Marking

Figure 11. *Device Marking. Top View.*

Ordering Information

To order, please order as specified below:

Product Name:	Intel Order Number:	Package Type:	Case Temperature Range:
GD16524-100BA	**FAGD16524100BA** MM#: 836092	100 pin TQFP	-40 ... 85 °C

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